UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JUNG-CHIH HUANG,
YISHAO MAX HUANG, BRIAN OH,
AND STERLING DU

Appeal No. 2006-1110
Application No. 09/429,174

HEARD: MAY 24, 2006

Before HAIRSTON, BLANKENSHIP, and SAADAT, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 18.

The disclosed invention relates to an integrated circuit pre-boot security controller that comprises a non-volatile password memory that stores at least one user password, a password input circuit for receiving a password, a digital logic circuit for comparing the password received by the password input circuit with the user password recorded in the password memory, and an output circuit coupled to the digital logic circuit for

transmitting an output signal to a power system to provide operating power to a digital computer.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. An integrated circuit pre-boot security controller adapted for inclusion in an electronic device that includes both a digital computer and a power subsystem for energizing operation of the digital computer, the pre-boot security controller receiving electrical power even though the power subsystem is not energizing operation of the digital computer and being adapted for enabling the power subsystem to energize operation of the digital computer upon receiving a pre-recorded user password by the pre-boot security controller, the integrated circuit pre-boot security controller comprising:

a non-volatile password memory that stores at least one user password;

a password input circuit for receiving a password that is to be compared with any user passwords recorded in said password memory;

a digital logic circuit for comparing the password received by said password input circuit with any user passwords recorded in said password memory if the pre-boot security controller is in a security operating mode; and

an output circuit that is coupled to said digital logic circuit for transmitting an output signal to the power subsystem that enables the power subsystem to energize operation of the digital computer if the password received by said password input circuit matches a user password recorded in said password memory.

The references relied on by the examiner are:

Lewis	4,604,708	Aug. 5, 1986
Sibigtroth et al. (Sibigtroth)	5,251,304	Oct. 5, 1993
Chao	5,313,639	May 17, 1994
Thandiwe	5,594,319	Jan. 14, 1997

Claims 1, 3, 4, 7, 8, 10, 12, 13, 16 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lewis in view of Sibigtroth.

Claims 2, 5, 9, 11, 14 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lewis in view of Sibigtroth and Thandiwe.

Claims 6 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lewis in view of Sibigtroth and Chao.

Reference is made to the final rejection, the briefs and the answer for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will sustain the obviousness rejections of claims 1 through 18.

According to the examiner's findings (final rejection, pages 3 and 4), Lewis discloses all of the structure of claims 1 and 10 except for the pre-boot security controller being implemented as an integrated circuit, and Sibigtroth discloses a controller and a memory as part of an integrated circuit package. Based upon the teachings of the references, the examiner stated "[i]t would be obvious to one skilled in the art to construct the

microcomputer of Lewis in the method of Sibitroth [sic, Sibigtroth] because it is more compact."

The appellants argue that there is a lack of a teaching, suggestion or motivation to combine the teachings of the references in the manner suggested by the examiner, and that such combined teachings would leave the PROM 34 in Lewis outside the integrated circuit (brief, pages 18 through 22). Appellants question whether size of the components is a problem in either Lewis or Sibigtroth, and question whether size of the components provides adequate motivation for modifying the teachings of Lewis (brief, pages 23 and 24). Appellants also argue (brief, pages 44 through 48) that the declaration submitted by Brian Oh[1] proves that the Lewis system modified in accordance with the teachings of Sibigtroth would be vulnerable to attack by a thief.

In response to appellants' arguments, the examiner provided additional clarification that "Sibigtroth teaches it is desirable to build a controller and memory, including non-volatile memory, on an integrated circuit package (Sibigtroth Col 2 lines 19-25)," and that "[i]t would be obvious to one skilled in the art to integrate the controller and memory of Lewis on the specific integrated circuit structure of Sibigtroth because of its small size, decreased access and increased security" (answer, page 7).

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1 Brian Oh is a co-inventor of the subject application.

We agree with the examiner's finding that Sibigtroth describes an integrated circuit package that includes a data processor 14, a memory 13 and a non-volatile memory in programmable security device 20 (Figure 1; column 1, lines 14 through 19; column 2, lines 18 through 25; column 3, lines 33 through 39; column 4, lines 1 through 6 and 55 through 60). The Background of the Invention in Sibigtroth clearly explains that space on a single-chip integrated circuit is limited because of the small size of the integrated circuit chip, and that individual circuit components on the chip have to be small in size because of the limited space on the integrated circuit chip. In view of the recognition by Sibigtroth that savings in space can be achieved by placing circuit components (e.g., a data processor and memories) on a single-chip integrated circuit, we agree with the examiner that it would have been manifestly obvious to the skilled artisan to use a single-chip integrated circuit with a data processor and memories as taught by Sibigtroth in lieu of the discrete data processor 10, ROM 32 and non-volatile memory 34 used by Lewis to save space in the electronic device. See In re Kahn, 441 F.3d 977, 988, 78 USPQ2d 1329, 1337 (Fed. Cir 2006), wherein the Court stated "the 'motivation-suggestion-teaching' test asks not merely what the

references disclose, but whether a person of ordinary skill in the art, possessed with the understandings and knowledge reflected in the prior art, and motivated by the general problem facing the inventor, would have been led to make the combination recited in the claims." Stated differently, the motivation, suggestion or teaching may be implicit from the prior art as a whole, rather than an explicit statement in the prior art. WMS Gaming, Inc. v. International Game Tech., 184 F.3d 1339, 1355, 51 USPQ2d 1385, 1397 (Fed. Cir. 1999). Accordingly, we find that the single-chip integrated circuit saves space by networking the formerly discrete components on the single chip. Thus, appellants' arguments to the contrary notwithstanding, the examiner did not have to resort to impermissible hindsight to demonstrate the obviousness of using a single-chip integrated circuit in lieu of discrete components to save space in the electronic device described by Lewis.

Appellants' argument that the PROM 34 in Lewis would be located outside the integrated circuit chip is without merit because Sibigtroth specifically teaches that the non-volatile memory (i.e., PROM) is part of the single-chip integrated circuit.

The evidence of non-obviousness submitted by the declarant assumes that the skilled artisan would bodily incorporate the circuit structure disclosed by Sibigtroth into the electronic device described by Lewis. The test for obviousness is not whether the features of the secondary reference may be bodily incorporated into the structure of the primary reference. Rather, the test for obviousness is what the combined teachings of the references would have suggested to the skilled artisan. In re Keller, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981).

The declarant's position that the Lewis device would be subject to attack by a thief or via a compromise in security is without merit in view of the fact that the Sibigtroth structure is not bodily incorporated into the Lewis electronic device. If the discrete devices described by Lewis are placed on a single-chip integrated circuit as taught by Sibigtroth, then the components would be protected by the chip packaging as in the disclosed invention. As a result of the chip packaging taught by the combined teachings of the references, appellants' argument (brief, page 48) that "the combined references teach away from the claimed invention because they leave the impression to one of ordinary skill in the art that their combination lacks the desired property of theft deterrence" is without merit.

In summary, the obviousness rejection of claims 1 and 10 is sustained. The obviousness rejection of claims 2, 3, 5, 9, 11, 12, 14 and 18 is likewise sustained because appellants have chosen to let these claims stand or fall with claims 1 and 10 (brief, Pages 19 and 20).

Appellants argue (brief, pages 25 through 28) that Lewis and Sibigtroth fail to disclose the security keypad of claims 4 and 13. We disagree with appellants' arguments. The keypad 24 and input line 25 to the microcomputer 10 is a security keypad in Lewis that operates like the security keypad in the disclosed and claimed invention. For this reason, the obviousness rejection of claims 4 and 13 is sustained.

Turning to claims 7 and 16, appellants argue (brief, pages 28 through 31) that neither Lewis nor Sibigtroth teaches or would have suggested a state machine. Appellants' arguments to the contrary notwithstanding, nothing in the claims precludes the microcomputer 10 and the program states in ROM 32 from operating in unison as a "state machine" as set forth in claims 7 and 16. Accordingly, the obviousness rejection of claims 7 and 16 is sustained.

Turning next to claims 8 and 17, we disagree with the appellants' argument (brief, pages 31 through 35) that the alarm

mode in Lewis is not an output as set forth in the claimed invention. We find that the output alarm in Lewis is an indication that a security operating mode exists in the electronic security system (column 2, lines 48 through 51). Based upon this teaching in Lewis, the obviousness rejection of claims 8 and 17 is sustained.

Turning lastly to claims 6 and 15, we find that the key pressings in Lewis are saved in memory so that the inputted code can be compared to the stored code. In view of the teachings in Lewis, the teachings of Chao are found to be merely cumulative to the teachings of Lewis. In summary, the obviousness rejection of claims 6 and 15 is sustained because we disagree with appellants' arguments (brief, pages 35 through 39).

DECISION

The decision of the examiner rejecting claims 1 through 18 under 35 U.S.C. § 103(a) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv).

AFFIRMED

KENNETH W. HAIRSTON
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

MAHSHID D. SAADAT
Administrative Patent Judge

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